A time and energy saving based frame adjustment strategy (TES-FAS) tag identification algorithm for UHF RFID systems

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***Abstract*—Radio frequency identification (RFID) is widely applied in massive items tagged domains. Existing medium access control (MAC) solutions primarily focus on improving slot efficiency or reducing the total number of slots. However, with pervasive applications of RFID, the time and energy consumption are increasingly important and should be considered in the new design. In this paper, we re-exam the problem of tag identification in UHF RFID system from the perspective of time and energy consumption. The presented work comprehensively reviews and analyzes the prior tag reading protocols. Based on prior art, we further discuss a novel design of tag reading algorithm to improve both time and energy efficiency of EPC C1 Gen2 UHF RFID standard. By exploring the effectiveness of embedding slot-by-slot mechanism in a sub-frame observation phase and combine the sub-frame and slot-by-slot observation in the proposed algorithm, which can achieve more fine-grained frame size adjustment with time and energy-efficiency. Moreover, the cardinality estimation function of the algorithm is implemented by the look-up tables, which allows dramatically reduction in computational complexity and energy consumption. Both simulation results and experiments show clear performance improvement over the commercial solutions.**

***Index Terms*—RFID, tag identification, EPC C1 Gen2, time efficiency, energy efficiency.**

I. Introduction

RADIO frequency identification (RFID) is an emerging wireless communication technology that can identify specific targets through radio signals without mechanical or optical contact, and has been applied in various applications including supply chain management, inventory control, logistics management, food traceability, and so forth [1-3]. Typically, an RFID system consists of a single reader, multiple tags, and a back-end subsystem. Tags are enclosed to the items with their IDs to be identified by the reader. A reader is either fixed or portable device. A shared wireless channel is used for communication between the reader and tags. The reader broadcasts the signal containing both continuous wave (CW) and modulated commands to tags. The tags energize themselves from reader's interrogating radio waves and responds to the reader according to the received command and executes data transmission by backscatter modulation.

RFID has many advantages, such as non-line of sight, multi-target identification, long lifetime, repeatable reading and writing, positioning and tracking [4]. For RFID reader, the main object is to collect tag information as quickly as possible. For passive UHF RFID such as EPC C1 Gen2 system [5], the typical operating range is from 1 to 12 m [6]. This coverage usually involves a number of tags potential to be read at the same time by the reader. However, if more than one tag respond to the reader simultaneously, a collision may happen incurring a mixture of scattered signals, and thus lead to increase in identification delay of the RFID system. Consequently, RFID systems require to employ an efficient tag anti-collision protocol (also called tag identification algorithm) to coordinate the communication between reader and tags so that all tags can be successfully identified. In the past decade, the reading efficiency is the primary concern in anti-collision algorithms. However, with the wide-ranging deployment of handheld readers in practice, energy consumption becomes a vital issue. Energy efficient RFID protocol not only extends the operating life of reader and tags (if they are battery powered), but also promotes the growth of RFID in various applications that have been envisaged [7].

The prior art includes probabilistic and deterministic anti-collision algorithms. Existing probabilistic algorithms are consist of either Aloha-based [7-8] or tree splitting (TS)-based [9-11], which have been widely used in EPC C1 Gen2 or ISO/IEC 18000-6B. In TS, the reader continuously splits the concurrent tag group into smaller subsets. Although the TS algorithm inherits certain properties of the probabilistic

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algorithm, it is not sensitive to tag cardinality as the Aloha-based algorithms because the splitting probability for collided tag set is constant to 0.5 regardless of tag cardinality. However, it has relatively long identification latency especially when the tag population size is large. Moreover, running such algorithm is time-consuming because it has to retransmit the entire tag ID during collision arbitration. Furthermore, TS algorithm is not compatible with the current mainstream UHF standard, i.e., EPC C1 Gen2. ABS and FSA-CSS are TS-based solutions that are designed for continuous tag identification [11]. A recent collision bit identification and tracking technology [12] which allows a reader to identify the location of collided bits is proposed and widely used in the popular representative of deterministic algorithms, i.e., query tree (QT) algorithm [13-14]. In a QT-based algorithm, all tags maintain a unique ID. In each slot, the reader broadcasts a binary string to allow the tags to reply to it if the tag's ID prefix matches the string sent by the reader. If a collision occurs, the reader updates two new strings by appending a 0 and 1 at the end of the previous string and pushes them in the stack. The reading process is terminated until the stack is empty. The previous work on the QT-based algorithm focuses on how to update the probe string effectively and reduce the number of queries under the stationary scenario. However, in UHF RFID systems, there may be a large deviations in the backscatter link frequency of various tags, such collision bit identification and tracking technology with strict synchronization requirements is difficult to be implemented in UHF RFID [5][15-18].

As a contrary, DFSA algorithm is more favored by many commercial off-the-shelf products and has been standardized in the EPC C1 Gen2 and ISO/IEC 18000-7 [19]. The UHF RFID standard EPC C1 Gen2 specifies a series of commands to support the implementation of anti-collision protocols. The reader broadcasts a ***Query*** command to start an identification process. The ***Query*** command contains a key parameter Q whose value is from 0 to 15 and represents the frame size $F = 2^Q$ (i.e., the number of slots available in a frame). As a Query command is received, each tag randomly generates a 16-bits random number (named RN16) and extracts a Q-bit from RN16 as the tag's slot counter T_{sc}. The value of T_{sc} is decreased by one as a ***QueryRep*** command is received. When $T_{sc} = 0$, the tag responds to the reader with ID information. For a given slot, there are three outcome: singleton slot (only one tag response), collision slot (more than one tag responses), and empty slot (no tag response). EPC C1 Gen2 specifies an in-frame adjustment of frame size by using ***QueryAdj*** command. Specifically, if a collision slot is detected, the reader increases the value of Q by 1. If an empty slot is detected, the reader decreases the value of Q by 1. And if a singleton slot is detected, the reader keeps Q unchanged. Although Q-algorithm is simple to implement in RFID system, the detailed adjustment strategy is not explained in EPC C1 Gen2. Most RFID manufacturers currently comply with the EPC C1 Gen2 standard, promoting the research of DFSA algorithms [20-22]. Intuitively, DFSA protocol follows EPC C1 Gen2. But the difference is that DFSA algorithm adds an estimation function, that is, after the reading of the frame, a new frame size is set according to estimation result of tag cardinality. The general working flowchart of DFSA is illustrated in Fig. 1. However, the DFSA algorithms with high computational complexity are not suitable for low-cost readers. Recently, many DFSA work has been presented to reduce computational overhead. To reduce the estimation cost, an efficient anti-collision algorithm with early adjustment of frame length (EACAEA) is presented [23]. EACAEA is viewed as an improved version of FEIA. Since the estimation and frame size determination depends on one examination of a frame at a specific time slot during each identification round, it can achieve a good compromise between computational complexity and reading performance. The authors in [24] introduced an Improved Linearized Combinatorial Model (ILCM) to calculate the tag population size by using linear function. The function parameters can be obtained with moderate mathematical operations. However, its reading performance fluctuates sharply with the number of remaining tags because the ILCM adopts a frame-by-frame (FbF) based cardinality estimation. To achieve the robust performance, the slot-by-slot (SbS) version of ILCM has been presented in [25]. The literature [26] presented a method (named ABIAC) to identify the time slot distribution selected by the tags in advance, and hence to reduce the number of total slots by skipping empty slots. The ABIAC assumed that the number of tags approximately equal to the initial frame size, which is a strong assumption. In addition, ABIAC requires the reader to know the slot distribution before the end of current round of identification. However, both tag IDs and cardinality are unknown to the reader. Therefore, such skipping mechanism is very difficult to be implemented in current RFID standard.

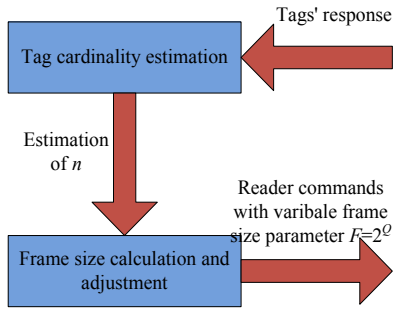

Fig. 1. The DFSA protocol for reader operation

The tag reading protocols based on sub-frame estimation strategy [27-28] are proposed to reduce the overall estimation error. The SUBF-DFSA [27] algorithm fully explores the linear relationship between the empty slot statistics and the collision slot statistics when the desired slot efficiency is satisfied. And then the linear relationship is used to estimate the remaining number of tags. In [28], a dynamic sub-frame based maximum a posteriori probability (DS-MAP) method is proposed to enhance the estimation accuracy and hence to improve the reading performance. To cease the estimation errors, the DS-MAP will return to conventional DFSA when it finds an appropriate frame size. Although the sub-frame based algorithms can improve the reading performance, their slot efficiency still below the upper bound (among implementable EPC C1 Gen2-based algorithms) of 0.368. For the purpose of breaking through the performance bottleneck of DFSA

algorithms, a partition based anti-collision algorithm named detected sector based DFSA (ds-DFSA) is proposed [29]. The highest slot efficiency of ds-DFSA peaks at 0.41. However, such algorithm requires an additional costs for existing commercial RFID platforms and therefore cannot be directly applied into off-the-shelf RFID systems. Although the above solutions focus mainly on how to reduce the number slots to read all tags, the setting of frame size, which also affects DFSA performance, has been ignored by these algorithms.

The key limitations of prior Aloha-based solutions are threefold. Firstly, to improve the estimation accuracy of the tag cardinality, most previous algorithms incur high computational overhead because they need to ensure the estimation accuracy. However, the anti-collision solutions with complex estimation are difficult to implement to low-cost reader (e.g., mobile or handheld reader) due to its constrained computational ability. Secondly, the reading performance of DFSA depends on both the cardinality estimation and the frame setting. However, the previous research is to optimize the frame size for maximum slot efficiency or minimal number of total slots, but in the actual scenario, time efficiency or energy efficiency are more important metric to evaluate the anti-collision algorithms [30-31]. The setting of frame size for optimal time and energy efficiency have been ignored by prior solutions. Finally, to improve the performance of tag identification, many previous algorithms try to modify the physical layer structure of the reader or tag, which is not compatible with existing EPC C1 Gen2 UHF RFID standard. However, all UHF RFID manufacturers strictly follow the EPC C1 Gen2 standard. Therefore, these solutions are difficult to implement on the EPC C1 Gen2.

To tackle the above limitations, we present an anti-collision solution called time and energy saving based frame adjustment strategy (TES-FAS) algorithm. The proposed algorithm integrates the low-cost estimation method, adaptive frame size calculation and efficient frame size adjustment policy. To be specific, the presented algorithm ascertains the optimal frame size based on both estimated cardinality, time parameters and energy efficiency of RFID system. Moreover, the proposed in-frame observation mechanism combines the sub-frame and slot-by-slot observation, which can early terminates the improper frame in a better manner. The main contributions of this paper are summarized as follows.

1) A time and energy saving based frame adjustment strategy (TES-FAS) algorithm is proposed to improve the time and energy efficiency by optimizing parameters that is not leveraged by the prior algorithms. The optimal parameter settings of the proposed TES-FAS algorithm are thoroughly investigated in order to maximize its performance.

2) The performance of the proposed TES-FAS algorithm is thoroughly evaluated on an off-the-shelf UHF RFID system following the EPC C1 Gen2 standard and is compared to commercial solutions. The experiment results show that the proposed TES-FAS is a suitable candidate for commercial RFID systems.

The rest of this paper is organized as follows. Section II describes the novel anti-collision algorithm named TES-FAS. The performance results have been illustrated in Section III. Section IV provides the experimental results in a real-world testbed and compares them with the off-the-shelf RFID systems. Finally, we conclude this paper in Section V.

II. Algorithm Description

A. Tag Cardinality Estimation

In the Aloha-based anti-collision algorithm, the performance depends on the frame setting (frame size is set closing to the tag number). However, in most RFID application scenarios, the number of tags remains unknown to the reader in advance, hence it is necessary to predict the number of tags in order to maximize the performance of the algorithm. Most existing DFSA solutions estimate the cardinality according to mathematical methods. As discussed above, such approaches incur higher computational costs. In our previous works [27-28], another type of estimation strategy based looking-up tables (LUT) is presented for reducing computational complexity. In this paper, we also refer to the LUT idea and design an efficient estimation method with low computational cost. Before describing the detailed estimation method, we firstly derive the relations of the number of empty slots and collision slots. Let P_E and P_C denote the probability of empty and collision of a slot within in a frame, respectively. It is concluded that the slot efficiency (U) is a convex function, where P_E and P_C are monotonically decreasing and increasing functions, respectively. It is proved that the optimal DFSA can asymptotically attain the highest slot efficiency of 0.368, given that the frame size equals to the number of tags [32]. The relation between the optimal frame size and tag cardinality range can be derived by the existing works [27-28][33]. We thus make a reasonable assumption to ensure a high average slot efficiency U, i.e., $U \geq 0.35$, and calculate the relation between the number of empty slots and that of collision slots for different frame size and estimated tag cardinality. The results are summarized in Tab. I and the deduce process can be found in the preliminary result [27]. Where N_e and N_c denotes the number of empty and collision slots within a frame.

TABLE I
The Relation Between N_e And N_c For Different Values of Frame Size And Cardinality

Estimated tag cardinality	Relation between P_E and P_C
$n_{est} = F_{cur}/2$ $(C_f = -1)$	$3.2N_c < N_e \leq 15.1N_c$
$n_{est} = F_{cur}$ $(C_f = 0)$	$0.6N_c < N_e \leq 3.2N_c$
$n_{est} = 2 * F_{cur}$ $(C_f = 1)$	$0.08N_c < N_e \leq 0.6N_c$

Most existing estimation approaches calculate the estimated cardinality and update the next frame size according to the statistical information in the foregoing full frame. However, once the previous frame is improper, the estimation error will be accumulated and causes the performance degradation. To overcome the impact of cumulative error on overall performance, the sub-frame observation is presented for adjusting frame size. Since a sub-frame is fraction of an original full frame, the ratio between the probability of empty and collision of a slot during a sub-frame equals to the ratio during the full frame. Therefore, the results in Tab. II can be used for both full frame and sub-frame. According to the results in Tab. I,

we can derive the following two simple rules to determine frame size.

1) Rule 1: if $N_e - 3.2N_c > threshold$, the reader terminates the ongoing frame and doubles the frame size.
2) Rule 2: if $N_e - 0.6N_c < -threshold$, the reader terminates the ongoing frame and shortens the frame size by two times.

These two rules help the reader decide whether the current frame is appropriate. Every time after reading a sub-frame, the reader will use them for judgment. Below, we describe the proposed estimation strategy. Here we refer to the maximum a posteriori probability (MAP) to calculate the tag cardinality based on the statistics from a sub-frame. Although MAP has been proven to improve estimation accuracy, it requires a high computational complexity impeding its application in low-cost RFID platforms. In the proposed estimation strategy, the LUT is also used to pre-store intermediate variable of estimation results. Since the size of the sub-frame and the number of items in the pooled table are strictly constrained, the designed estimation method is space-efficient and implementable. Considering that n tags fall into F slots, the probability that the empty slot appears N_e times, singleton slot appears N_s times, and collision slot appears N_c times in a sub-frame can be calculated by using multinomial distribution, which can be given as

$$P\left(n|N_e,\ N_s,\ N_c\right) = \frac{F_{sub}!}{N_e!N_s!N_c!} \cdot P_E^{N_e} P_S^{N_s} P_C^{N_c} \tag{1}$$

where F_{sub} is the size of the sub-frame, P_E, P_S, and P_C are the probabilities of empty, success and collision for a given slot in the full frame, respectively. The tag cardinality involved in a sub-frame is determined when the value of $P\left(n|N_e,\ N_s,\ N_c\right)$ is maximized. Thus, the estimated cardinality in a sub-frame is $\hat{n}_{sub}$. Then the estimated cardinality involved in the full frame is calculated as

$$\hat{n}_{est} = \hat{n}_{sub} \cdot \frac{F}{F_{sub}} \tag{2}$$

The estimated number of tags calculated by the sub-frame is directly stored in the LUT, thus avoiding real-time calculations in the estimation phase, thereby shortening the time cost of the estimation. Although the proposed estimation strategy requires additional storage space to store the LUT, it can use the sub-frame structure to limit the table size. The setting of sub-frame size should also be seriously considered. If a sub-frame size is too large, the reader requires more storage space to accommodate the LUT. On the contrary, the cumulative estimation error may be high which makes improper frame size determination when the sub-frame size is too small. Referring to our previous works [27-28], we recommend sub-frame size as listed in the Tab. II. For the purpose of controlling estimation error when the sub-frame size is small, we limit the frame size adjustment as $8 \times F_{sub}$. Also, since each estimation result of a LUT is stored in one Byte, its value cannot exceed 255. The maximum occupied memory size of LUTs can be calculated as $64 \times 65/2$ Bytes when the sub-frame size is equal to 64. Since five LUTs ($F_{sub} = 4,\ 8,\ 16,\ 32,\ 64$) are used in the estimation phase, the total storage space to accommodate them can be calculated as 2790 Bytes. Considering a handheld RFID reader embedded with ARM processor, such as AT91SAM256 with 256 Kbytes of internal high-speed flash, there is sufficient storage memory to store the required LUTs [27].

TABLE II
THE RECOMMENDATION SETTING OF F_{sub}

F	**8∼16**	**32∼64**	**128∼256**	**512∼1024**	**>1024**
F_{sub}	4	8	16	32	64

B. Adaptive Frame Size Calculation (Optimal Time Efficiency)

Existing solutions update a frame size according to the proximal value of estimated cardinality [7-8][22][24-28], and its slot efficiency is defined as the ratio between the number of tags and the total number of slots required to identify them. Such frame size update strategy is only feasible and reasonable when all types of time slots have equal durations. Obviously, it is a very strong assumption. The EPC C1 Gen2 standard has clarified the specific durations of an empty, a singleton, and a collision slot, as T_e, T_s, and T_c, respectively. Thus, the slot efficiency metric is not the best indicator to measure RFID reading performance. Moreover, such metric does not consider the time and energy consumption. Unlike the previous DFSA solutions, the proposed scheme updates the frame size by maximize the time efficiency and energy efficiency, respectively. Referring to our previous work, the time efficiency T_{effi} can be defined as

$$T_{effi} = \frac{S \cdot T_{EPC}}{T_{slots} + T_{FLOP}} \tag{3}$$

$$T_{slots} = S \cdot T_s + E \cdot T_e + C \cdot T_c \tag{4}$$

herein E, S, and C denote the number of empty, singleton and collision slots during a whole identification process, respectively. T_{EPC} denotes the time required for a tag to transmit a EPC (UID). T_s, T_e, and T_c denote the time interval of a singleton slot, empty slot and collision slot and have

$$\begin{aligned} T_s = {} & T_{cmd} + 2\left(T_1 + T_2\right) + T_{RN16} \\ & + T_{ACK} + T_{PC+EPC+CRC} \end{aligned} \tag{5}$$

$$T_e = T_{cmd} + T_1 + T_3 \tag{6}$$

$$T_c = T_{cmd} + \left(T_1 + T_2\right) + T_{RN16} \tag{7}$$

where T_{cmd} is the time duration taken by the anti-collision command sent by the reader, which can be Query, QueryAdj, or QueryRep [27]. T_{FLOP} represents the time cost due to the floating pointing operation of the estimation function and is expressed as

$$T_{FLOP} = \frac{\left(\sum_{i=1}^{N_{sw}} N_{FLOP}^i\right)}{R_{FLOPS}} \tag{8}$$

where N_{sw} is the number of rounds included in the entire identification process, which is counted by the reader. Consider a handheld or mobile RFID reader with a single-core ARM processor, its floating pointing operation (FLOP) ability is

strictly limited compared to multiprocessor which is equipped in smart phones or laptops. In our proposed anti-collision solution, FLOP cost is a key factor needs to be taken into account. It is also an important factor in measuring computational complexity, time efficiency and energy efficiency. The higher the computational complexity, the larger the value of N^i_{FLOP}, which represents the FLOP cost required by the reader during the i-th identification round. R_{FLOPS} denotes the computing power of k MFLOPS (10^6 FLOP per second).

Assuming that the tag population size to be identified is n and the initial frame size is set to F, the identification problem can be equivalent to a probability distribution in which r tags fall within a certain time slot with a probability of $1/F$, which can be expressed as

$$P_r = C^r_n \left(\frac{1}{F}\right)^r \left(1 - \frac{1}{F}\right)^{n-r} \tag{9}$$

Accordingly, $P_E = P_{r=0}$, $P_S = P_{r=1}$, and $P_C = P_{r>1}$ are the corresponding probabilities that a slot is empty, singleton, and collision, respectively. If the frame size F is assumed large enough, the probability distribution of r tags fell in a slot can be approximated as Poisson distribution with mean $\lambda = n/F$ [34]. Then, E, S, and C in Eq. (4) can be approximated as the functions of the tag number n and frame size F, which are given as

$$E = F \cdot P_E = F\left(1 - \frac{1}{F}\right)^n \approx F \cdot e^{-\lambda} \tag{10}$$

$$\begin{aligned} S = F \cdot P_S &= F \cdot \tfrac{n}{F}\left(1 - \tfrac{1}{F}\right)^{n-1} \\ &\approx F \cdot \lambda \cdot \left(\tfrac{F}{F-1}\right) e^{-\lambda} \end{aligned} \tag{11}$$

$$C = F \cdot P_C = F \cdot (1 - P_E - P_S) \tag{12}$$

Substitute Eqs. (10-12) into Eq. (3), the T_{effi} can be approximated as

$$T_{effi} \approx \frac{F \cdot T_{EPC} \cdot \lambda e^{-\lambda}}{T_{FLOP} + F\left(e^{-\lambda}\left(T_E + T_S \cdot \lambda - T_C - \lambda \cdot T_C\right) + 1\right)} \tag{13}$$

Taking the first derivative of the above formula with respect to λ, and making it equals to zero, we then obtain the Eq. (14)

The simple bisection or Newton's methods can be used to solve the above non-linear equation of one variable, and transforming the Eq. (14), we can have

$$e^{\lambda}(\lambda - 1) = \frac{F(T_e - T_c)}{T_{FLOP} + T_c \cdot F} \tag{15}$$

By solving the Eq. (15), the value of λ to maximize the time efficiency can be expressed as

$$\lambda_{TE} = 1 + W\left(\frac{F \cdot (T_e - T_c)\, e^{-1}}{T_{FLOP} + T_c \cdot F}\right) \tag{16}$$

where $W(*)$ is a Lambert W-function. Since $\frac{d^2 T_{effi}}{d\lambda^2} < 0$, consequently, the optimal setting of the frame size based on time efficiency can be given as

$$F^{TE}_{opt} = \frac{\hat{n}_{est}}{\lambda_{TE}} \tag{17}$$

C. Adaptive Frame Size Calculation (Optimal Energy Efficiency)

Energy efficiency is another important metric when implementing an RFID identification protocol to the systems where battery-powered reader is used. This section discusses the impact of frame size setting and estimation complexity on the energy-efficiency of the proposed algorithm. Referring to the definition of time efficiency, the energy efficiency is defined as

$$\eta_{effi} = \frac{S \cdot ((P_{Rt} + P_{Rr})\, .T_{EPC})}{T_{slots} \cdot P_{Rt} + T_{received} \cdot P_{Rr} + E_{est}} \tag{18}$$

where P_{Rt} and P_{Rr} respectively indicate the transmitted power and the received power of the reader during it identifies the tags. E_{est} is defined as the energy consumed by the reader during the estimation phase. $T_{received}$ denotes the total time that the reader is in the receiving mode during the identification process, which can be expressed as

$$T_{received} = C \cdot T_{RN16} + S \cdot (T_{RN16} + T_{EPC}) \tag{19}$$

herein T_{RN16} denotes the time duration of a 16-bits random number. Similarly, η_{effi} can also be approximated as the function of λ, which is written as

$$\eta_{effi} = \frac{F \cdot T_{EPC} \cdot \lambda \cdot (P_{Rt} + P_{Rr})}{C_1 \cdot e^{\lambda} + C_2 \cdot \lambda + C_3} \tag{20}$$

where C_1, C_2 and C_3 are the corresponding coefficients, and can be expressed as

$$C_1 = (E_{est} + P_{Rr} \cdot T_{RN16} + T_c \cdot F \cdot P_{Rt}) \tag{21}$$

$$C_2 = P_{Rr} \cdot T_{EPC} + F \cdot P_{Rt}\,(T_s - T_c) \tag{22}$$

$$C_3 = F \cdot P_{Rt}\,(T_e - T_c) - P_{Rr} \cdot T_{RN16} \tag{23}$$

Taking the first derivative of the Eq. (20) with respect to λ, and making it equals to zero, we then further have Eq. (24) where A_1, A_2 and A_3 are respectively written as

$$A_1 = E_{est} + T_c \cdot F \cdot P_{Rt} + P_{Rr} \cdot T_{RN16} \tag{25}$$

$$A_2 = F\,(P_{Rt} + P_{Rr}) \tag{26}$$

$$A_3 = F \cdot P_{Rt}\,(T_e - T_c) - P_{Rr} \cdot T_{RN16} \tag{27}$$

Adopting the similar method used to solve Eq. (14) , and transforming the Eq. (24), we can have

$$\left(T_{EPC} \cdot e^{\lambda} - \lambda\right) = -\frac{A_3}{A_1} \tag{28}$$

By solving the Eq. (28), the value of λ to maximize the energy efficiency can be calculated as

$$\lambda_{EE} = \frac{A_3}{A_1} - W\left(0,\ -T_{EPC} \cdot e^{A_3/A_1}\right) \tag{29}$$

where $W(*)$ is a Lambert W-function. Since $\frac{d^2 \eta_{effi}}{d\lambda^2} < 0$, consequently, the optimal setting of the frame size based on time efficiency can be given as

$$F^{EE}_{opt} = \frac{\hat{n}_{est}}{\lambda_{EE}} \tag{30}$$

$$\frac{dT_{effi}}{d\lambda} = \frac{F\left(F \cdot T_{EPC} \cdot (T_e - T_c) - T_{EPC} \cdot e^{\lambda}\left(T_{FLOP} + T_c \cdot F\right)(\lambda - 1)\right)}{\left(T_{FLOP} \cdot e^{\lambda} - F\left(T_c\left(e^{\lambda} - 1 - \lambda\right) - T_s \cdot \lambda - T_e\right)\right)^2} = 0 \tag{14}$$

$$\frac{d\eta_{effi}}{d\lambda} = \frac{A_1 A_2\left(e^{\lambda} T_{EPC} - \lambda\right) + A_2 A_3}{\left[A_1 e^{\lambda} + \left(F \cdot P_{Rt}\left(T_s - T_c\right) + P_{Rr} \cdot T_{EPC}\right)\lambda + A_3\right]^2} = 0 \tag{24}$$

D. Frame Size Adjustment

Since DFSA algorithms do not maintain a constant frame size for the entire identification process, rather, updates it dynamically. Therefore, the reader should examine whether the current value is appropriate or not during the identification process and decide if a new frame is required. Three main mechanisms of frame size adjustment can be found in the literatures. The first is Frame-by-Frame mechanism [22][24][33], which always updates a new frame at the end of the previous frame. In Frame-by-Frame (FbF) mechanism, when the frame size is much greater than the number of tags, its performance will drop dramatically. The second is Slot-by-Slot (SbS) [5][21][25][35-36], compared with the FbF strategy, the update frequency of frame size is fairly frequent because it calculates a new frame size at every slot of a frame. The SbS strategy suffers from a rather high complexity. The last is Point-by-Point (PbP) mechanism [23][26-28], where P is defined as the index value of a certain slot in a frame. The reader uses the time slots whose index value is less than or equal to P to update the frame size. However, in the previous works, the reader only specifies the initial values of F_{sub} corresponding to different frame size and is unable to adaptively update the F_{sub} size according to the state of the slots have been read. In our proposed algorithm, we adopt a hybrid frame updating mechanism combining PbP and SbS. In each slot, the reader will judge the relationship between N_e and N_c, and then update the frame size according to the difference between them. After the reading of F_{sub} slots, the reader estimates the tag cardinality and calculates the new frame size in the next identification round. Then the reader determines whether to enable the new frame according to the decision condition. The decision condition can be divided into two types: maximum time efficiency and maximum energy efficiency.

On the one hand, if the reader obeys to the maximum time efficiency mode, it will compute the time efficiency T_{effi1} and T_{effi2}, respectively, using the current frame size and the frame size that is expected to be updated. In order to maximize the time efficiency, a new frame will be enabled only if $T_{effi1} < T_{effi2}$. Otherwise the reader will continue to read the next time slot of the frame. On the other hand, if the reader obeys to the maximum energy efficiency mode, it will compute the corresponding η_{effi1} and η_{effi2}. On the other hand, a new frame will be enabled only if $\eta_{effi1} < \eta_{effi2}$. The reader terminates the entire identification process until no collision occurs. According the presented frame size setting policy, the reader ensures that if a frame is enabled at a pointer whose index equals to the value of F_{sub}, the expected time efficiency or energy efficiency will be improved.

By combining tag cardinality estimation and adaptive frame size calculation, time and energy saving based frame adjustment strategy (TES-FAS) algorithm is proposed. The pseudo-code of the proposed TES-FAS is described in **Algorithm 1**. where $threshold = Multiply \cdot Q$ is an upper value that allows the F_{sub} to be end in advance. If the relative number of N_e vs. the adjusted number of N_c falls within the $threshold$, the F_{sub} is unchanged. Otherwise, the reader ends the ongoing sub-frame. In our simulations and experiments, the $Multiply$ is set as 4.

Algorithm 1 TES-FAS Reader Operation

```
Initialize F_ini, F_sub, N_e, N_s, N_c, slot_index;
while C ≠ 0 do
    The reader identifies tags and counts (N_e, N_s, N_c) slot by slot;
    slot_index++;
    if N_e − 3.2N_c/λ > threshold then
        F_sub = slot_index;
    else if N_e − 0.6N_c/λ < −threshold then
        F_sub = slot_index;
    end if
    if slot_index == F_sub then
        Computes (T_effi1, T_effi2) or (η_effi1, η_effi2) according the system requirement;
        if T_effi1 < T_effi2 then
            Updates the new frame size according to (17) and updates corresponding F_sub;
        else if η_effi1 < η_effi2 then
            Updates the new frame size according to (30) and updates corresponding F_sub;
        else
            slot_index++;
        end if
    else
        slot_index++;
    end if
end while
```

III. Simulation Results

In this section, we compared the proposed TES-FAS with prior state-of-the-art solutions including MAP [22], ILCM [24], EACAEA [23], SUBF-DFSA [27], and Q-algorithm [5] (which is a standard DFSA solution specified by EPC C1 Gen2) over extensive Monte Carlo simulations. Simulation scenarios with a reader and a various number of tags have been evaluated using MATLAB 2012b. Since the practical environments have almost the same impact on the reference methods, the communication channel between the reader and tags are assumed to be ideal as in the literatures [21-28]. In

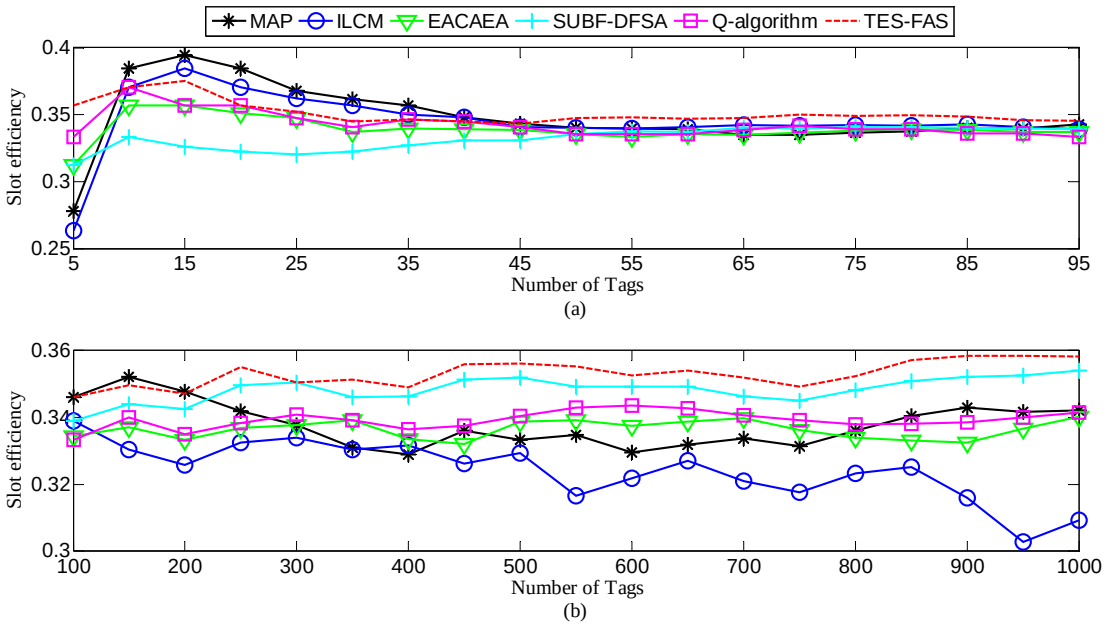

Fig. 2. The comparison of slot efficiency: (a) for $5 \leq n \leq 95$ (b) for $100 \leq n \leq 1000$

our simulations, the sparse mode refers to the number of tags from 5 to 95, and the dense mode refers to the number of tags from 100 to 1000. To reduce the randomness and ensure the convergence, the simulation results are average over 2000 iterations [7][11][34].

TES-FSA outperforms all other algorithms and achieves nearly 95.4% of optimal slot efficiency under sparse mode. TES-FSA also outperforms all other algorithms and achieves nearly 96% of optimal slot efficiency under dense mode. Fig. 2 (a) compares slot efficiency of various algorithms where the tag population size is from 5 to 95. The initial frame size is set to 16. As can be observed, the proposed TES-FAS algorithm achieves more stable performance, especially when number of tags increases. The slot efficiency of the six curves range from the lowest to the highest as follows: SUBF-DFSA, EACAEA, Q-algorithm, ILCM, MAP and TES-FAS. For ILCM and MAP, their slot efficiency is above 0.36 when the number of tags is around 15, and their slot efficiency decreases as the number increases. The reason is that their frame updating mechanisms are based on a single calculation from a full frame. When the actual number of tags approaches the frame size, they can achieve accurate estimation and hence obtain a good performance. Once the tag population size is away from the frame size, their slot efficiency drops dramatically. Hence, their performance shows obvious fluctuations. As a contrary, EACAEA, SUBF-DFSA can provide more stable performance than previous two algorithms by using PbP strategy to adjust the frame size. Although the performance of Q-algorithm is most stable by using SbS policy, its slot efficiency is lower than that of SUBF-DFSA and TES-FAS. Fig. 2 (b) presents the slot efficiency when the tag population size ranges from 100 to 1000. The frame size is also initialized as 16. By comparing both Fig. 2 (a) and (b), most of approaches show discrepant performance. For example, the average slot efficiency of SUBF-DFSA is lower than EACAEA, ILCM, Q-algorithm and MAP when the tag population size is from 5 to 95. However, as the tag population size increases, the impact of the initial frame size on performance will be weakened. The SUBF-DFSA can timely terminate the inappropriate frame through the PbP frame size updating mechanism, thereby suppressing its impact on performance as much as possible. Benefiting from the hybrid frame size adjustment strategy, the proposed TES-FAS can always maintain the best average performance compared to other algorithms.

As concluded in the previous works [27-28], the slot efficiency is ineffective to evaluate the actual performance of anti-collision algorithm because it assumes the duration of different types of slots are equal. Meanwhile, the slot distribution of various algorithms is different. Therefore, the time efficiency and energy efficiency are also taken into account in the simulations. To obtain the time efficiency, we need to measure the time duration of every step in Eqs. (5), (6), (7), and FLOP (8) used in the collision arbitration process. The primary time parameters are based on EPC C1 Gen2. To evaluate the FLOP cost of anti-collision algorithm, we use the reference values presented in our previous work [27]. Specifically, the FLOP cost of anti-collision algorithm derives from the cardinality estimation and frame size setting in the identification process. The higher the complexity of the estimation, the greater the cost the FLOP required. The same principle also applies to frame size setting. The parameters used to evaluate the time efficiency and energy efficiency in MATLAB simulation are summarized in Tab. III, where the power parameters are referred to [37].

The comparison of time efficiency is illustrated in Fig. 3. We can observe from Fig. 3 (a), the curves of all algorithms fluctuate when the tag population size is small. As the tag population size is greater than 35, their time efficiency grad-

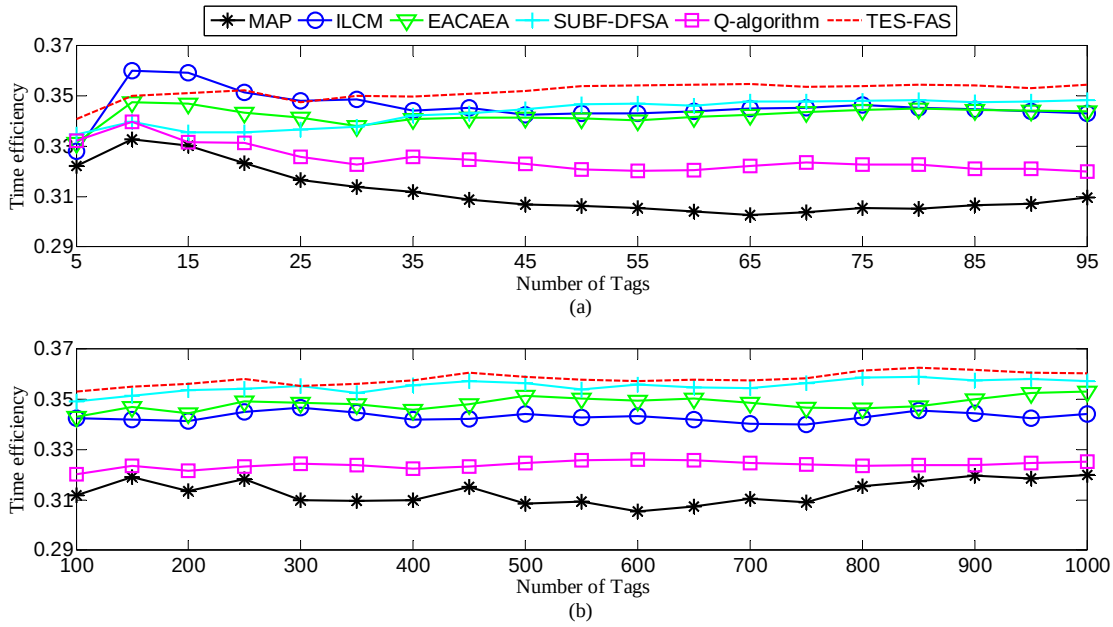

Fig. 3. The comparison of time efficiency: (a) for $5 \leq n \leq 95$ (b) for $100 \leq n \leq 1000$

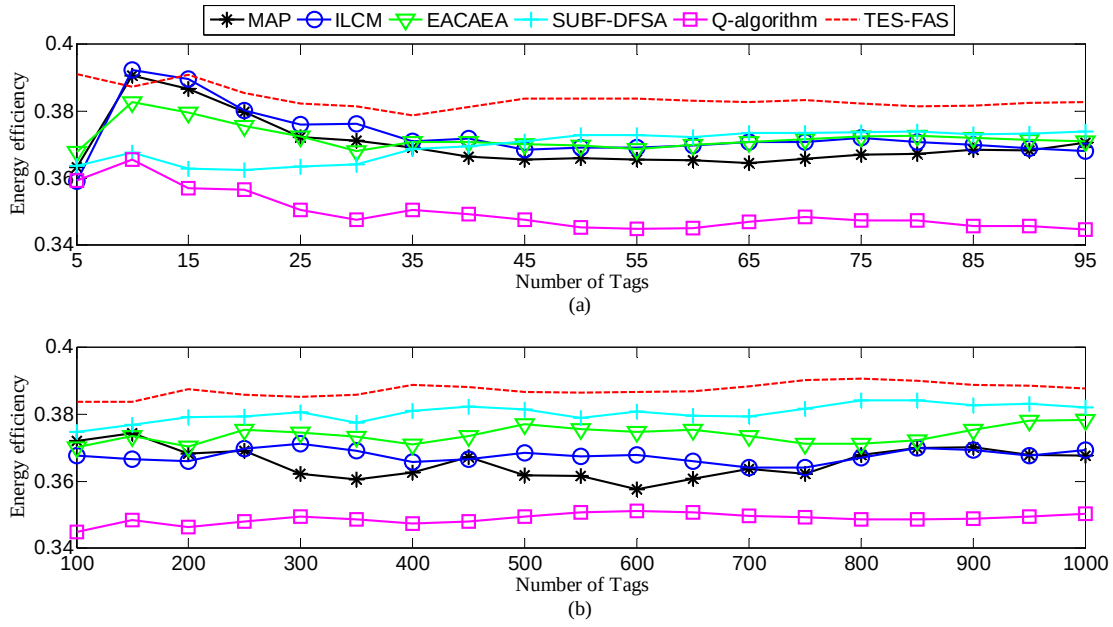

Fig. 4. The comparison of energy efficiency: (a) for $5 \leq n \leq 95$ (b) for $100 \leq n \leq 1000$

TABLE III
THE TIME PARAMETERS USED IN MATLAB SIMULATIONS

Parameters	Values
R->T Preamble	112.5 μs
Tari	12.5 μs
T->R Preamble	112.5 μs
BLF	160kHz
Data Coding	FM0
T1	62.5 μs
T2	62.5 μs
T3	50 μs
P_{Rr}	125 mW
P_{Rt}	825 mW

ually becomes stable, this is especially true when the tag population size is above 100 in Fig. 2 (b). Different from results in Fig. 2, all algorithms can achieve the highest time efficiency when the number of tags is around 10. However, with a continue increase of tag population, all algorithms show deteriorate performance because they need additional slots to estimate the population size of unread tags. It is also noted that the time efficiency depends on both time interval and estimation complexity, hence various algorithms show discrepant performance under such evaluation metrics. For example, the slot efficiency of MAP is higher than ILCM, whereas its time efficiency is lower than that of ILCM when

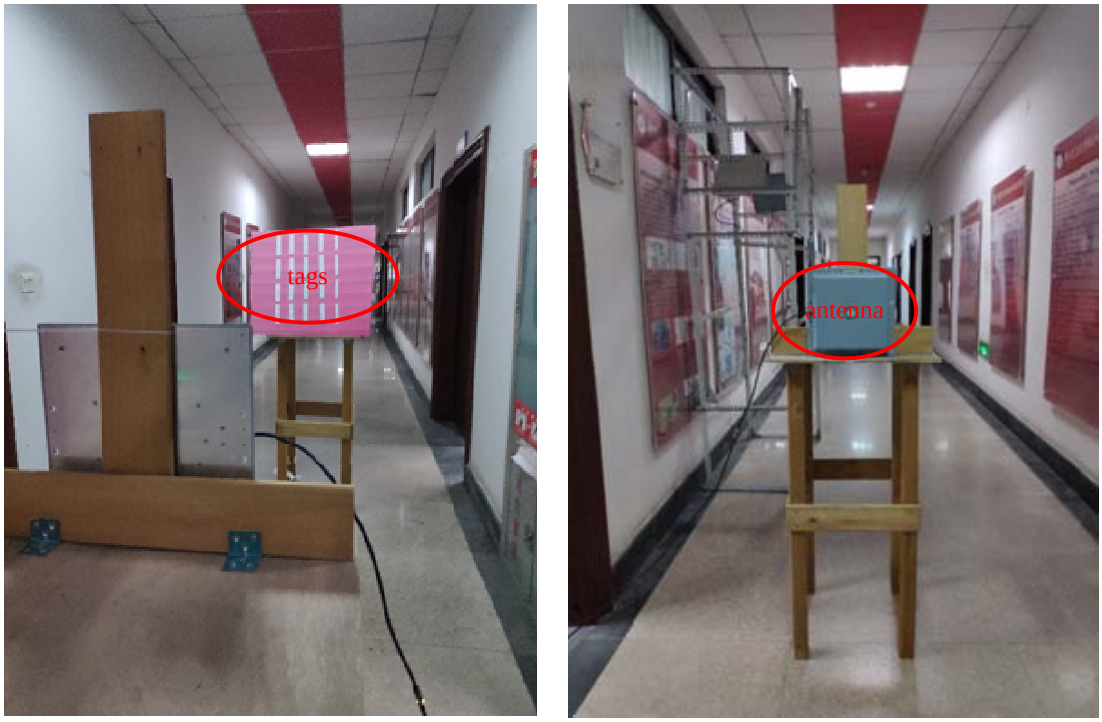

Fig. 5. The Experimental Environment of RFID Anti-collision

the number of identified tags is between 100 and 1000. The reason is that the estimation complexity of ILCM is much lower than that of MAP. Although the identification time T_{slots} of Q-algorithm is longer than that of MAP, its time efficiency is higher than MAP because the T_{FLOP} of MAP is greater than that of Q-algorithm. The proposed TSA-FAS maintains the best time efficiency by reducing the estimation complexity and optimizing the frame size. Specifically, its average time efficiency achieves 0.3583, which is 14.4% higher than MAP algorithm.

To further illustrate the advantages of TES-FAS, Fig. 4 compares the energy efficiency of various algorithms. We can observe from Fig. 4(a), the curves of all algorithms also fluctuate when the number of tags is from 5 to 45. As the tag number is above 45, their energy efficiency become more stable. As can be observed in Fig. 4(b), almost all approaches maintain a constant energy efficiency when the number of tags is between 100 to 1000. Different from the results in Fig. 3, some algorithms perform differently in terms of energy efficiency. For example, the time efficiency of Q-algorithm is higher than that of MAP algorithm. However, its energy efficiency is lower than MAP. Since the reader needs to frequently sends the QueryAdj command to update the frame size in Q-algorithm, its identification time T_{slots} is longer than MAP algorithm. Therefore, the total energy consumption of Q-algorithm is higher than that of MAP. The other algorithms maintain the same performance ranking in time efficiency metric. The proposed algorithm reduces both the identification time and estimation complexity, hence it can achieve the best performance in terms of slot efficiency, time efficiency and energy efficiency.

IV. Experimental Results With A Practical RFID Testbed

To evaluate the reading performance of the proposed TES-FAS solution in an off-the-shelf UHF RFID system, we conduct experiments with a testbed in an indoor environment. Experimental platform includes an active RFID reader and various commercial tags. The reader is equipped with AT91SAM7S256 microprocessor and Indy R2000 RF transceiver chip. Where AT91SAM7S256 is a 32-bit RISC microprocessor based on the ARM7TDMI core. The single-cycle access frequency is 30MHz, with 256KB Flash memory size and 64KB SRAM memory size on the chip. The Indy R2000 is an RFID reader chip for the UHF band produced by Impinj Inc. It has advantages of high performance, low power consumption and high receiving sensitivity, and can meet the demands of long-distance reading and multi-tag identification. The Indy R2000 reader chip integrates RF and baseband modules to receive data from compatible RFID tags, and is now widely used by industry and enterprise. For the convenience of description, the reader composed of AT91SAM7S256 microprocessor and Indy R2000 chip as core modules are collectively referred as R2000 reader, and the anti-collision strategy provided by Impinj Inc itself is named Impinj R2000 algorithm. The environment scenario used for experiments is captured in Fig. 5, where includes an R2000 reader, an antenna and 120 commercial tags.

Tab. IV lists the link parameters configured for radio frequency communication between the reader and tags. The experiments are carried out by placing 120 commercial tags in the RFID reader antenna interrogation zone with a fixed transmitting power. Note that in this paper, we only focus

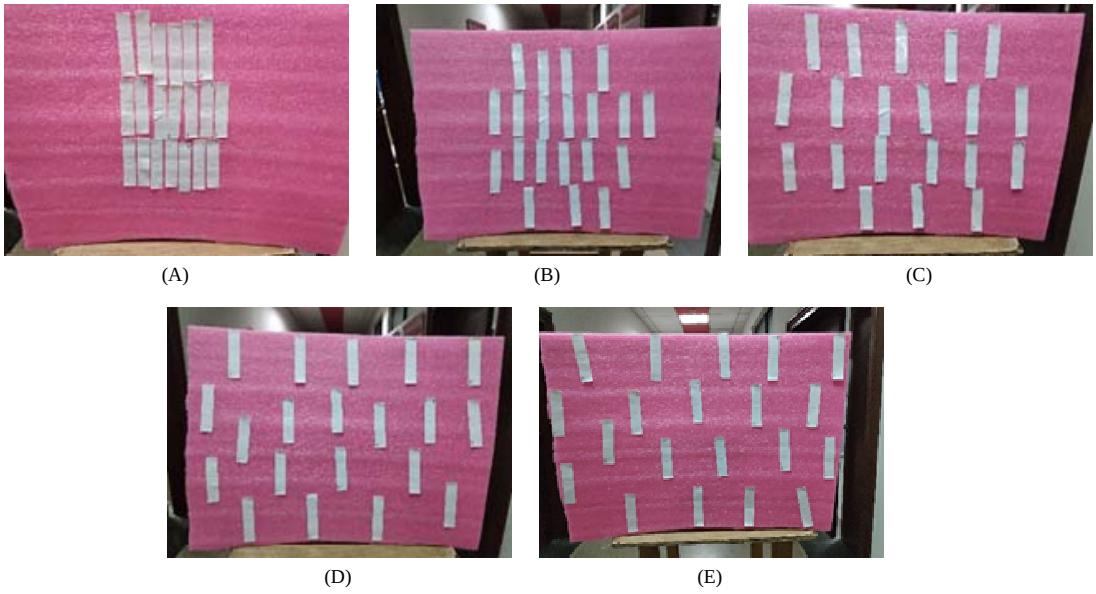

Fig. 6. Various Scenarios With Different tag-to-tag Distance

TABLE V
AVERAGE IDENTIFICATION RATE VS. DISTANCE

Distance	Average identification rate	Distance	Average identification rate
35cm	235.5 tags/s	1.7m	188.9 tags/s
55cm	232.4 tags/s	2.1m	176.3 tags/s
75cm	227.1 tags/s	2.5m	177.1 tags/s
1m	215.6 tags/s	3.0m	173.0 tags/s
1.3m	212.4 tags/s	4.0m	142.6 tags/s

TABLE IV
THE LINK PARAMETERS SETTING BETWEEN THE READER AND TAG COMMUNICATION

Experimental scenario	1	2
R->T Modulation	PR-ASK	DSB-ASK
R->T coding	PIE	PIE
Tari (textmu s)	25	25
PW (μs)	12.5	12.5
RTcal (μs)	62.5	75
TRcal (μs)	85.33	200
DR	64/3	8
T->R Modulation	Miller-4	FM0
TRExt	1	1
BLF (kHz)	250	40
Data Rate (kbps)	62.5	40

on the software level algorithm. The anti-collision protocol only specifies the data communication procedure between the reader and tags, and does not need to modify air interface of the existing EPC C1 Gen2 standard. Therefore, the proposed TES-FAS can be implemented in the protocol module of the reader firmware with C programmable language. The hardware level (e.e., how does the reader decode and what the sensitivity it is etc.) is out of the scope of this paper. We fixed the output power of the reader and changed the distance between the reader's antenna and tags (from 35cm to 4m). And then we recorded the average (tags/s) under different distances. The Tab. V summarizes the record of the Impinj R2000 reader by using the proposed TES-FAS. The results show that putting tags in the near field of the reader's antenna will not influence the reader's receiving sensitivity. However, in most applications, the tags are in the far field of the reader's antenna. To make our tests in line with practice, we fix the distance between the reader's antenna and tags to 1.3 m so that the tags are in the far field of the antenna. It is also noted that the distance between tags also affect the practical tests, we have to find out how far between tags can make such influence be negligible. Since influence between tags may be caused by many reasons, it is difficult to find out the optimal distance through theoretical calculating. We solve this problem by doing some experiments with different tag-to-tag distance. Five test scenarios are shown in Fig. 6. We keep the same distance between the tags and the reader's antenna. We record the average identification rate under these scenarios in the Tab. VI. From Tab. VI, we know that when tags are too close, the identification rate is negatively affected. When scenarios change from A to C, the identification rate improves. However, the identification rate does not have a visible change when the scenario changes from C to E, even though tags in D and E have a larger distance than C. That is to say, the distance between tags in C has already made the influence between tags negligible. Thus all our practical tests are conducted using the same gap as tag setup in C.

Fig. 7 shows the experimental results by using TES-FAS, Impinj R2000 and Q-algorithm to identify the same batch tags in the same time period under the experiment scenario 1.

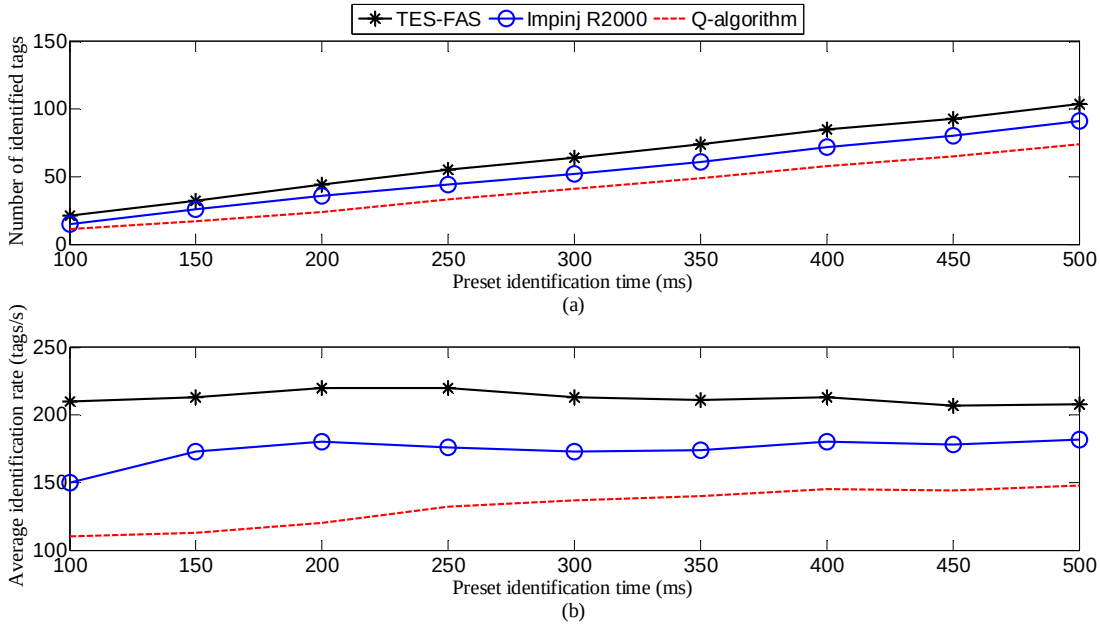

Fig. 7. Comparison of the experimental results under scenario 1: (a) number of identified tags (b) average identification rate

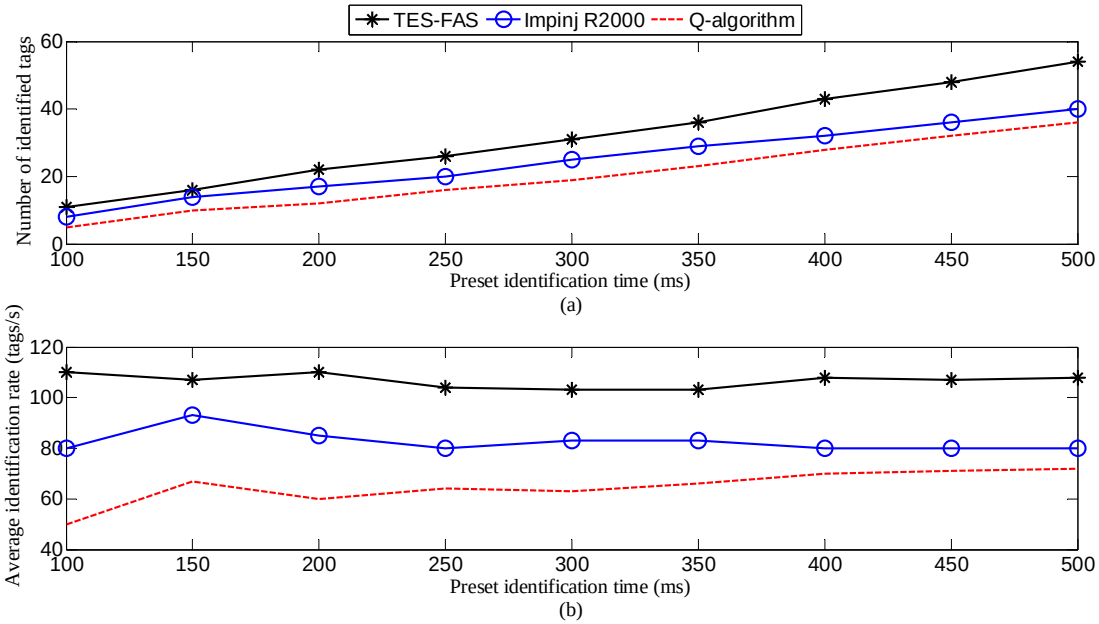

Fig. 8. Comparison of the experimental results under scenario 2: (a) number of identified tags (b) average identification rate

TABLE VI
COMPARISON OF AVERAGE IDENTIFICATION RATE UNDER DIFFERENT SCENARIOS

Different scenarios	Average identification rates (tags/s)
A (0.3cm)	169
B (1.5cm)	185
C (4cm)	210
D (6cm)	208
E (8cm)	213

As can be observed from Fig. 7 (a), the TES-FAS algorithm can identify more tag numbers in the given time period. As the preset identification time increases, the performance advantages of the TES-FAS become more and more obvious. For example, the TES-FAS identifies 85 tags when the preset identification time is 400 ms, whereas the Impinj R2000 and Q-algorithms identifies 72 and 58 tags, respectively. As illustrated in Fig. 7 (b), the proposed TES-FAS improves the average identification rate (which is defined as the number of identified tags per unit time) by 22.4% compared to Impinj R2000.

The experimental results under scenario 2 are compared in Fig. 8. As can be seen, the performance of all algorithms deteriorates sharply when adopting FM0 coding. The number

of identified tags in the unit time is significantly lower than that in Miller coding. In addition, when using Miller coding, the anti-interference ability is strong and the reader side is more likely to recover the tag signal, thereby ensuring better communication quality between the reader and tags. No matter what coding method is used, the proposed TES-FAS always hold the best performance, which improves the average identification rate by 28.9% compared to Impinj R2000. Both simulation and experiment results indicate that the proposed TES-FAS outperforms the Impinj R2000 constantly in practical RFID system.

V. Conclusion

We have focused on the time and energy efficiency of DFSA algorithm in RFID tag identification, and a novel DFSA-based tag identification algorithm namely TES-FAS has been proposed for EPC C1 Gen2. Unlike conventional DFSA methods, the TES-FAS reduces the cardinality estimation complexity by using LUT and allows the frame size to be adaptively configured according to different parameters setting. Benefiting from such adaptive frame setting mechanism and low cost cardinality estimation strategy, the TES-FAS has been shown to improve the reading performance without any modification on hardware level. The simulation results have shown that TES-FAS outperforms prior art in terms of slot efficiency, time efficiency, and energy efficiency. We have also prototyped a RFID system and the experimental results show that compared to the commercial solution, the proposed TES-FAS improves the average identification rate by 22.4% and 28.9% respectively under different experiment scenarios. The promising experimental results indicate that the proposed TES-FAS is a suitable candidate for the commercial and industrial RFID systems.

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