An Effective Frame Breaking Policy for Dynamic Framed Slotted Aloha in RFID

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***Abstract*—Tag collision problem is considered as one of the critical issues in RFID system. To further improve the identification efficiency of UHF RFID system, a frame breaking policy is proposed with dynamic framed slotted aloha algorithm. Specifically, the reader makes effective use of idle, successful and collision statistics during the early observation phase to recursively determine the optimal frame size. Then the collided tags in each slot will be resolved by individual frames. Simulation results show that the proposed algorithm achieves a better identification performance compared with the existing Aloha-based algorithms.**

***Index Terms*—RFID, anti-collision, Aloha, identification rate.**

I. Introduction

ULTRA high frequency (UHF) RFID is widely used for auto identification as a replacement of the barcodes because of its contactless nature with more convenience and efficiency. A typical RFID system is composed of a reader and multiple tags [1]. Fast identification is an urgent demand for a RFID system especially in densely tagged environments, such as warehouse and supply chain management. Therefore, an effective anti-collision algorithm is important in accelerating tag identification. To cope with the multiple tags identification, many anti-collision algorithms have been proposed, which can be classified into Aloha-based [2-4], query tree (QT)-based [5], and hybrid algorithms [6-7].

Technically, QT-based algorithm is considered as a deterministic method derived from a collision bit identification and tracking technique. However, along with the increasing number of tags, the position of collision bit cannot be detected efficiently since the wide deviation of received signals [8-9] at a reader in UHF RFID system. Therefore, it is difficult to implement QT-based algorithms or hybrid algorithms which adopt bit tracking technology in UHF RFID systems.

In this paper, we focus on Aloha-based methods, which are widely used in UHF RFID systems. As the tag backlog (unread tags) is unknown for a reader, an estimation method is required for an anti-collision algorithm. To ensure the accuracy of tag backlog estimation, most previous methods [3-4] require a large computation overhead. However, most RFID readers are embedded with only a single-chip microprocessor with limited computation capability. As a result, estimation methods with high computation overhead are inefficient in terms of identification time/rate.

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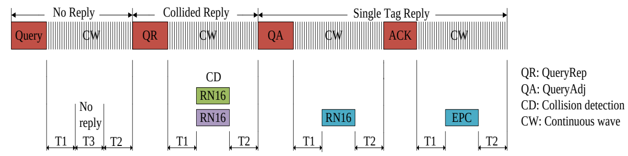


Fig. 1. Link timing between a reader and tags

Recently, many state-of-art works [10-11] have presented energy efficient algorithms for the purpose of low computation overhead. The author in [10] introduced a feasible and easy-to-implement anti-collision algorithm (FEIA). However, the performance will be largely limited if the initial slot is idle during a frame. The literature [11] proposed an Improved Linearized Combinatorial Model (ILCM) that only incurs a modest calculation cost, and can be easily implemented as a tag backlog estimation method. Nonetheless, its performance deteriorates when the number of tags varies in a large scale.

To reduce the computation complexity and improve the identification performance of Aloha-based algorithms, we propose an effective frame breaking policy named detected sector based dynamic framed slotted Aloha (ds-DFSA) for the EPC C1 Gen2 standard [9]. Specifically, the proposed algorithm determines the optimal frame size based on the observation of a fraction of current frame. If the current frame size is not optimal, the reader will end the current identification round and adjust a new frame size for the next round. Otherwise, the identification round will continue, and the collided slots will be resolved by individual frames. The simulation results shows that the proposed scheme can achieve much better system efficiency, shorter identification time and higher identification rate than the other Aloha-based algorithms.

II. System Model and Algorithm Description

A. The optimal frame size setting for a tag backlog

DFSA is the most prevalent version of Aloha-based algorithm to deal with multiple tags collision. The system transmission model between a reader and tags is illustrated in Fig. 1. Where T1 is the time from reader transmission to tag response, T2 is the reader response time required if a tag is to demodulate the reader's signal, T3 is the time that a reader waits, after T1, before it issues another command.

In DFSA, the reader broadcasts an initial frame size and adjusts it according to the estimated backlog at the end of each identification round. The tags randomly select a slot during a frame and respond to the reader. Consider n tags waiting to be identified during the operation range of a reader with a frame size F, the system efficiency can be written as [3]

$$U = (n/F) * (1 - 1/F)^{n-1} \tag{1}$$

The maximum efficiency can be obtained when the frame size equals to the number of tags ($F = n$). Since the number of tags is unknown for the reader, most existing algorithms focus on the tag backlog estimation. These methods adjusts the frame size according to the observation of the previous full frame. However, once the previous frame size is inappropriate, the system efficiency will be degraded. The standard such as EPC C1 Gen2 specifies an in-frame adjustment of frame size by using **QueryAdj** command. The main advantage of Q-algorithm is that an identification process will be end if the reader detects an inappropriate frame size. However, the adjustment strategy is not explained in details.

We first derive the optimal number of tags for each frame size. Since the system efficiency U is a convex function of the number of tags n and frame size F [3], the critical value n^* to adjust the frame size should have the system efficiency of a frame size F_L (F_L=2^Q) equals to that of a frame size F_H (F_H=2^{Q+1}). Therefore, according to Eq. (1), we have

$$n^* = 1 + ln\left(\frac{F_H}{F_L}\right) / ln\left(\frac{F_L}{F_H} \cdot \frac{F_H - 1}{F_L - 1}\right) \tag{2}$$

Since the number of tags n must be an integer in a practical RFID system, we can derive the following optimal frame size mapping to a tag backlog

$$F = \begin{cases} 2^Q, & for\ n = \lfloor n^* \rfloor \\ 2^{Q+1}, & for\ n = \lceil n^* \rceil \end{cases} \tag{3}$$

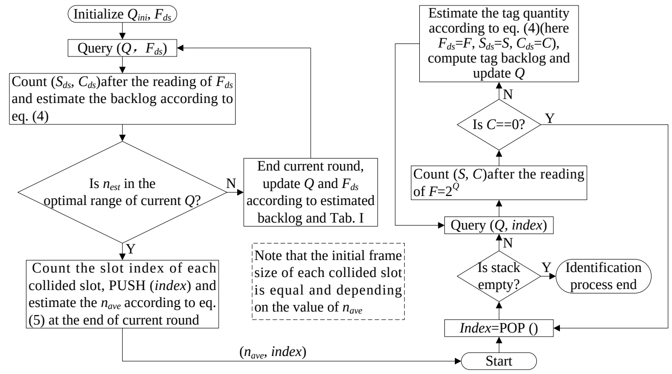
where $\lfloor * \rfloor$ and $\lceil * \rceil$ represent round down and round up to the nearest integer, respectively. According to Eqs. (2) and (3), the optimal frame size for all tag backlog can be derived. It is noted that the authors in [12] provide another Q-selection method with can yield the same result. But our scheme is simpler without multiple loop iterations.

B. The backlog estimation method

To obtain the tag backlog, an efficient and simple estimation method is required to avoid large computation. According to Schoute's method [2], the estimated tag quantity of a full frame can be given as $n_{est} = S + 2.39C$, where S and C are the number of successful and collision slots at the end of current identification round. Different to the existing solutions [3][11-12] where the tag quantity is estimated by the previous full frame, we propose an algorithm to estimate the tag quantity by only using a fraction (also called detected sector F_{ds}) of the current frame. The estimated tag quantity can be given as

$$n_{est} = (S_{ds} + 2.39 \cdot C_{ds}) \times F/F_{ds} \tag{4}$$

where S_{ds} and C_{ds} are the number of successful and collision slots during the detected sector. F_{ds} is the size of the detected sector. Since F_{ds} is the proportion of the current full frame, it varies during the identification process. According to the estimation result from (4), the reader ends the current identification round if the n_{est} is not in the optimal range of current frame size. That is to say, an identification round with a new frame size and detected sector is required. The above process will be repeated until detecting a proper frame size. Noting that n_{est} may be zero when the frame size is much greater than the number of tags. In this case, the estimated tag backlog denotes $F/4 - S_{ds}$. It is noted that since F_{ds} is only a small proportion of the full frame size, the estimation error has the negligible impact on the whole performance. After several estimation during identification rounds, the reader can adjust an appropriate frame size fit for the backlog. Derived from extensive simulations, Tab. I summarizes the recommendation setting of F_{ds} for different F.



(a) Optimal frame size detection (b) Individual identification for each collided slot

Fig. 2. The flowchart of the proposed ds-DFSA

TABLE I
THE RECOMMENDATION SETTING OF F_{ds}

F	**8**	**16**	**32∼128**	**256∼512**	**1024**	**>1024**
F_{ds}	$F/2$	$F/4$	$F/8$	$F/16$	$F/32$	$F/64$

C. The proposed algorithm ds-DFSA

After detecting an appropriate frame size, the reader continues the current identification round and estimates the average number of collided tags in collision slots at the end of this round. The average number of tags in a collision slot can be estimated as

$$n_{ave} = \lfloor (n_{est} - S) / C \rfloor \tag{5}$$

where $n_{est} - S$ is the estimated tag backlog, C is the number of collision slots. Then, the reader queries each collided slot with an optimal frame depended on the value of n_{ave}. Combining backlog estimation method and frame size setting, Fig. 2 shows the flowchart of ds-DFSA, in which F_{ds} should be set as $F/2^k$ (k is an integer), i.e., $F/2$, $F/4$, $F/8$, etc., since the size of full frame F is 2^Q (Q is an integer from 0 to 15). The minimum of F_{ds} should be 2, since F_{ds} should be power of 2 and contain at least a collision and successful slot to estimate backlog according to (5). It is worth noting that the identification process for each collided slot is the same as that of traditional DFSA. Hence, ds-DFSA will not bring in extra cost compared to the traditional DFSA.

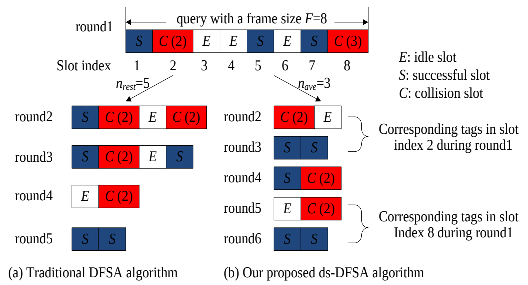


Fig. 3. An identification example of ds-DFSA

lemma 1. *Under the perfect condition (the unidentified tags are known for the reader), $U_{ds-DFSA} > U_{DFSA}$, where DFSA includes FEIA, MAP, ILCM and Q-algorithm.*

Proof: As the number of tags is known for the reader, the optimal frame size (the number of slots) is equal to the tag backlog during each identification round. After reading the initial frame F, the reader counts the number of collision slots m and each slot contains k_i ($k_i \geq 2$) tags. Since the system efficiency (1) can be redefined as the number of tags divided by the total number of slots that identify all tags, we can have:

$$U_{DFSA} = n/\left(F + A\right) \tag{6}$$

where $A = n_{rest}/(1 - 1/n_{rest})^{n_{rest}-1}$ is the expected slots to identify n_{rest} tags according to Eq. (1), $n_{rest} = \sum_{i=1}^{m} k_i$ is the number of unidentified tags. With the same conditions, we can derive the system efficiency of ds-DFSA as

$$U_{ds-DFSA} = n/\left(F + B\right) \tag{7}$$

where $B = \sum_{i=1}^{m} \frac{k_i}{(1-1/k_i)^{k_i-1}}$. Assuming k_l is the largest of all k_i, we have $B < B^* = \frac{\sum_{i=1}^{m} k_i}{(1-1/k_l)^{k_l-1}}$, since the function of $(1 - 1/k)^{k-1}$ is a decreasing function. Therefore, we have $U^*_{ds-DFSA} = n/\left(F + B^*\right) > U_{DFSA} = n/\left(F + A\right)$ because n_{rest} is greater than k_l. As a result, $U_{ds-DFSA} > U^*_{ds-DFSA} > U_{DFSA}$. □

It is noted that Lemma1 shows the upper bound performance of ds-DFSA under perfect condition. Simulation results are also supplemented to verify the effectiveness of the proposed solution in both perfect and imperfect conditions.

We also provide an illustrated example in Fig. 3 to further explain the process of the proposed ds-DFSA algorithm. Assume there are eight tags which wait to be identified, and the initial frame size is 8. The traditional DFSA algorithm estimates the backlog according to the total number of collision slots and then adjusts the new frame size to fit the backlog. As a contrary, the ds-DFSA assigns the frame with small size for each collision slots. As can be observed in Fig. 3, the ds-DFSA consumes less slots than the traditional DFSA. Further advantage can be achieved when the number of tags increase.

III. Simulation Results

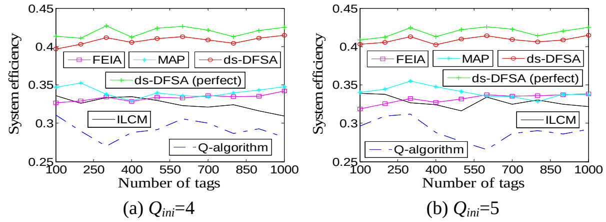
We evaluate the system efficiency, average coordination time for one tag identification and identification rate (the number of tags identified per second), and compare its performance with existing methods including Maximum a posteriori estimation (MAP) [3], FEIA [10], ILCM [11], and Q-algorithm [9] over extensive Monte Carlo simulations. According to the EPC C1 Gen2 specification, the primary time parameters are listed in Tab. II.

TABLE II
The Simulation Parameters According to EPC C1 Gen2

Parameters	value	Parameters	value
Reader-to-tag data-0	1Tari	RTcal	37.5μs
Reader-to-tag data-1	2Tari	TRcal	50μs
Reader-to-tag rate	80kbps	T1	62.5μs
Tag-to-reader rate	160kbps	T2	62.5μs
Tpri	6.25μs	T3	50μs
Tari	12.5μs	RN16	16bits
DR	8	EPC	128bits
Query	22bits	Ack	18bits
QueryAdj	9bits	QueryRep	4bits

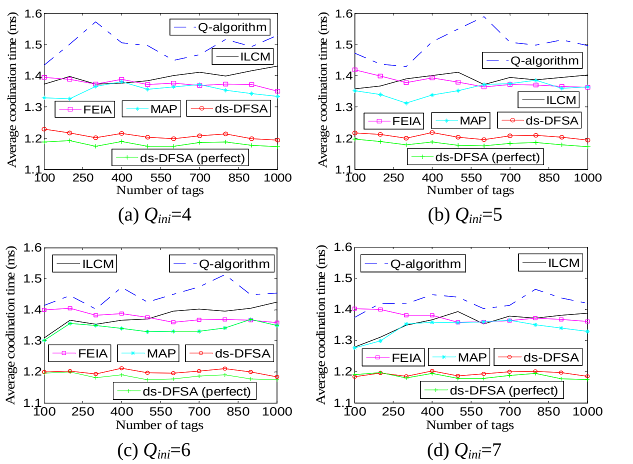
We first compare the system efficiency of various algorithms with different initial frame size ($F = 2^Q$) in Fig. 4. As can be seen from Fig. 4, the performance of Q-algorithm, MAP and ILCM are significantly affected by the initial frame size. When the number of tags is large and the initial frame size is small, these methods are unable to adjust to an appropriate frame size to fit the tag backlog, and cause performance deterioration. In other words, the stability and scalability of these methods are poor to adapt to a wide range of the number of tags. Compared to Q-algorithm, MAP and ILCM, the system efficiency of FEIA is almost independent to the initial frame seize, which means FEIA can efficiently adapt the frame size to the current tag backlog benefiting from its slot-by-slot adjustment strategy. However, the performance of FEIA is lower than that of MAP which adopts an extensive computation to achieve a higher performance. Moreover, the efficiency of FEIA is also lower than that of ILCM when the number of tags is relatively small. This is because the algorithm estimates the tag backlog slot by slot and uses the observation from previous slots. When the number of previous slots is small, the estimation becomes inaccurate and thus affects the identification performance. Also can be observed from Fig. 4, the efficiency of ds-DFSA is always better than that of other methods. The average efficiency of ds-DFSA is about 0.41 which is above the maximum system efficiency of existing DFSA algorithms.

Note that the total time for identifying tags consists of the necessary time for valid data (such as EPC or ID) transmission and coordination time such as the time duration of commands, guard time, etc. To obtain the total and coordination time required to identify all tags, the time intervals of each slot type and commands used in the identification process should be computed. The time parameters referring to EPC C1 Gen2 standard are listed in Tab. II. Fig. 5 shows the simulation results of average coordination time required to identify one tag. As can be found from Fig. 5, the proposed ds-DFSA algorithm spends average 1.2033 millisecond (ms) coordination time to identify one tag when the number of tags varies from 100 to 1000 in step of 100 with an initial Q_{ini} of 4, 5, 6, and 7,



(a) Q_{ini}=4 (b) Q_{ini}=5 (c) Q_{ini}=6 (d) Q_{ini}=7

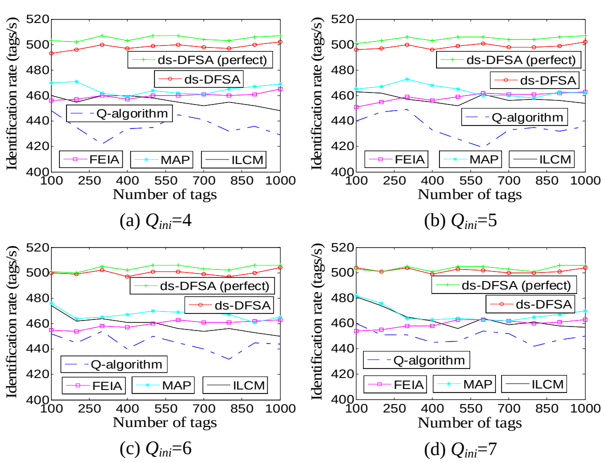
Fig. 4. Comparison of system efficiency



(a) Q_{ini}=4 (b) Q_{ini}=5 (c) Q_{ini}=6 (d) Q_{ini}=7

Fig. 5. Comparison of average coordination time for one tag identification

whereas Q-algorithm, ILCM, FEIA and MAP spend 1.4746, 1.3846, 1.3783, and 1.3542 ms, respectively. The ds-DFSA consumes less coordination time than other algorithms.



(a) Q_{ini}=4 (b) Q_{ini}=5 (c) Q_{ini}=6 (d) Q_{ini}=7

Fig. 6. Comparison of average identification rate

The average identification rate under different Q_{ini} is illustrated in Fig. 6. Specifically, the average identification rate of ds-DFSA is about 499 (tags/s). Due to the reduction in coordination time, the proposed ds-DFSA can achieve higher identification rate than other methods. That is to say ds-DFSA can identify more tags per unit time. To fully show the reliability of various performance metrics, we define the fluctuating function

$$f = (S_{TD}/M_{ave}) \tag{8}$$

where S_{TD} and M_{ave} denote the standard deviation and mean value of variables, respectively. f indicates the performance fluctuation. With a smaller f, a better reliability can be achieved. Tab. III compares the reliability of system efficiency, coordination time for identifying one tag, and identification rate when the number of tags varies from 20 to 1000 in step of 20 with an initial Q_{ini} of 4, 5, 6, and 7, respectively. As can be observed from Figs. 4-6 and Tab. III, the ds-DFSA can achieve the best overall performance. Also, since our proposed algorithm is based on the same hardware platform of Q-algorithm, it will not bring in extra requirements compared to other algorithms.

TABLE III
COMPARISON OF RELIABILITY OF VARIOUS PERFORMANCE METRICS

Methods	System efficiency	Coordination time	Identification rate
Q-algorithm	f=7.06%	f=7.43%	f=3.69%
ILCM	f=5.94%	f=6.13%	f=2.93%
MAP	f=5.36%	f=5.99%	f=2.76%
FEIA	f=1.80%	f=1.22%	f=0.77%
ds-DFSA	f=2.01%	f=1.31%	f=0.75%

IV. CONCLUSION

In this letter, we proposed an efficient anti-collision algorithm for identifying multiple RFID tags within the reader field. The proposed scheme determines the optimality of the current frame size based on the observations of detected sector, and then assigns small-size frames for each collided slot if the current frame is optimal. Through theoretical analysis and simulation results, we show that our schemes can achieve the better performance.

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